20 V P-Channel NexFET™ Power MOSFET

Check for Samples: CSD25402Q3A

FEATURES

- **Ultra-Low Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Low $R_{DS(on)}$**
- **Pb and Halogen Free**
- **RoHS Compliant**
- **SON 3.3 mm × 3.3 mm Plastic Package**

APPLICATIONS

- **DC-DC Converters**
- **Battery Management**
- **Load Switch**
- **Battery Protection**

DESCRIPTION

This –20 V, 7.7 mΩ NexFET™ power MOSFET is designed to minimize losses in power conversion load management applications with a SON 3 × 3 package that offers an excellent thermal performance for the size of the device.

PRODUCT SUMMARY

V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	7.5		nC
Q_{gd}	Gate Charge Gate to Drain	1.1		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V	74	mΩ
		V_{GS} = –2.5 V	13.3	mΩ
		V_{GS} = –4.5 V	7.7	mΩ
V_{th}	Threshold Voltage	–0.9		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25402Q3A	SON 3 × 3 Plastic Package	13-inch reel	2500	Tape and Reel

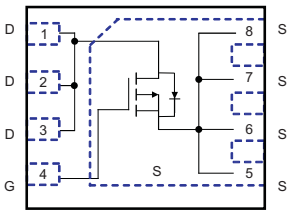
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	+12 or –12	V
I_D	Continuous Drain Current, T_C = 25°C	–72	A
	Continuous Drain Current (Package Limit)	–35	A
	Continuous Drain Current(1)	–15	A
I_{DM}	Pulsed Drain Current(2)	–82	A
P_D	Power Dissipation(1)	2.8	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

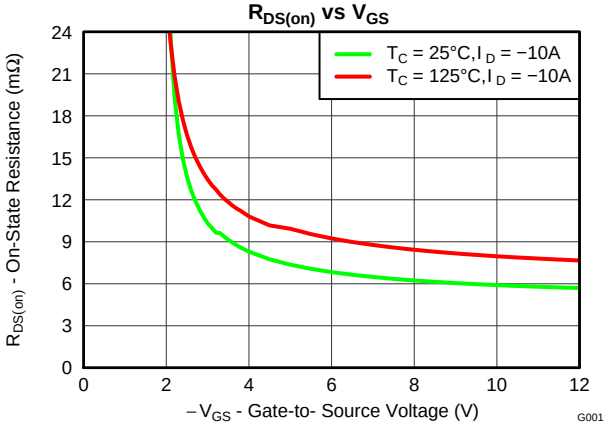
(1) $R_{\theta JA}$ = 55°C/W on 1 inch² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300 µs, duty cycle ≤2%

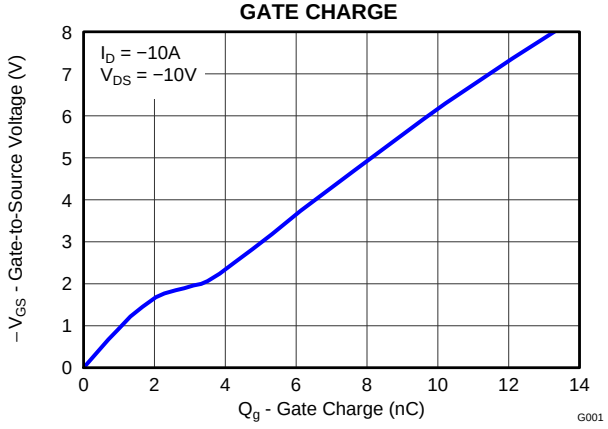
Top View



$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

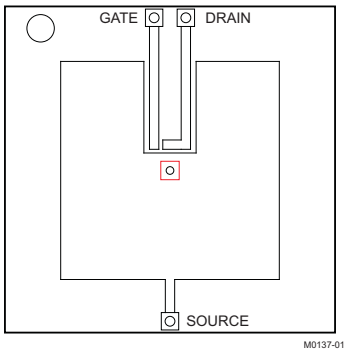
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 µA	–20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±12 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.65	–0.90	–1.15	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V, I_D = –1 A		74	300	mΩ
		V_{GS} = –2.5 V, I_D = –10 A		13.3	15.9	mΩ
		V_{GS} = –4.5 V, I_D = –10 A		7.7	8.9	mΩ
g_{fs}	Transconductance	V_{DS} = –10 V, I_D = –10 A		59		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		1380	1790	pF
C_{OSS}	Output Capacitance			763	992	pF
C_{RSS}	Reverse Transfer Capacitance			39	51	pF
R_G	Series Gate Resistance			3.7	7.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = –10 V, I_D = –10 A		7.5	9.7	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			2.4		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.0		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		7.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –10 A , R_G = 5 Ω		10		ns
t_r	Rise Time			7		ns
$t_{d(off)}$	Turn Off Delay Time			25		ns
t_f	Fall Time			12		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = –10 A, V_{GS} = 0 V		–0.8	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS} = –8.5 V, I_F = –10 A, di/dt = 200 A/µs		10.3		nC
t_{rr}	Reverse Recovery Time			21		ns

THERMAL CHARACTERISTICS

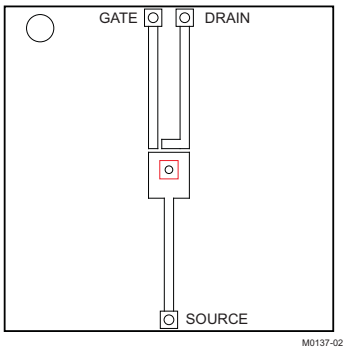
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			2.3	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			55	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 55°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 175°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

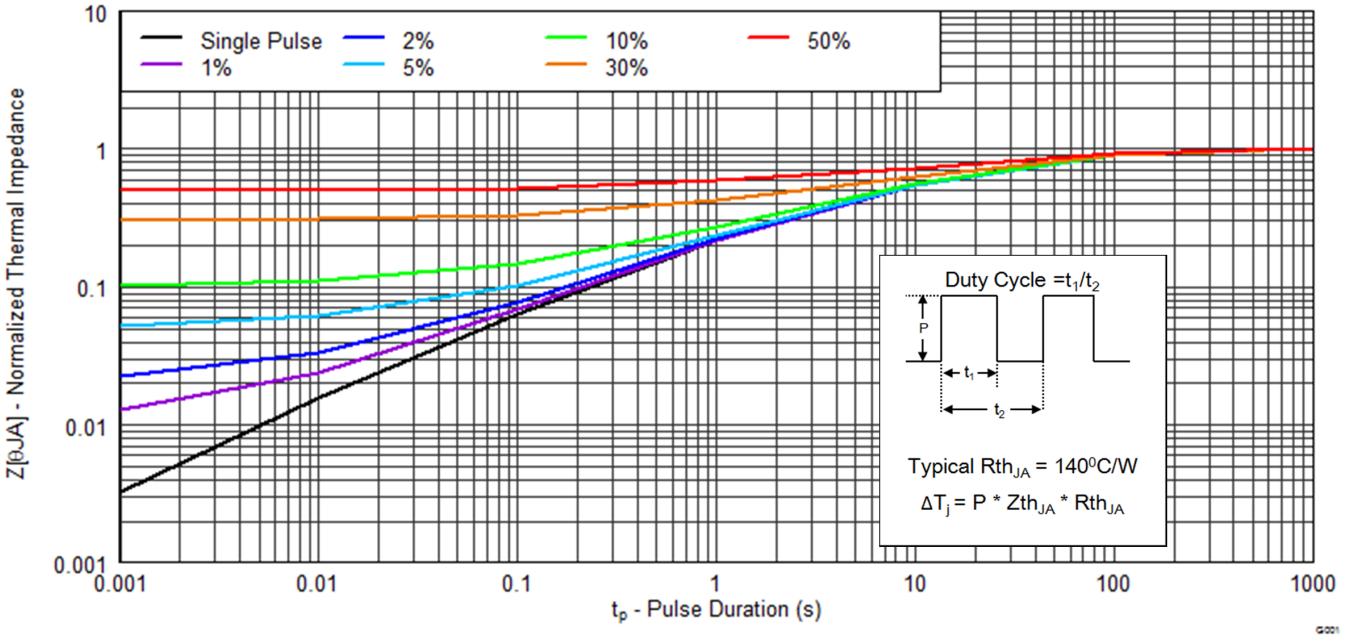


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

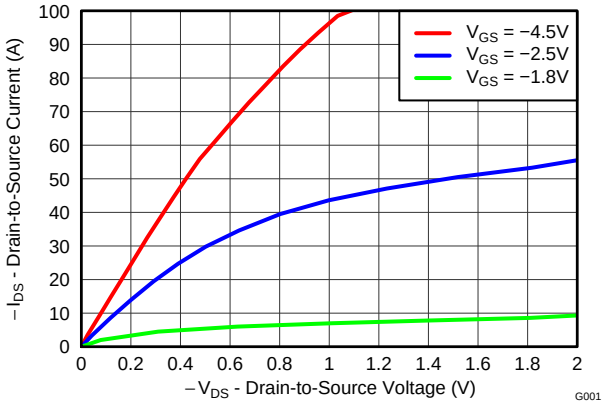


Figure 2. Saturation Characteristics

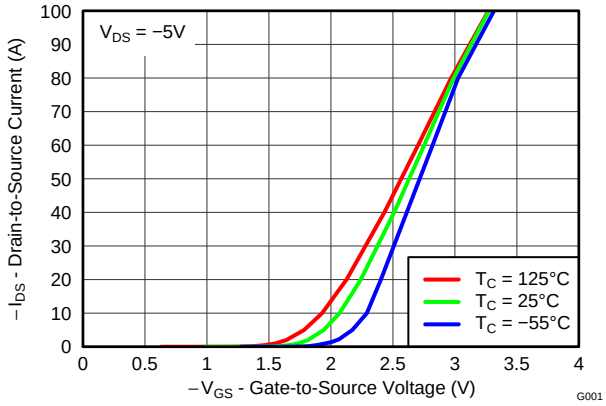


Figure 3. Transfer Characteristics

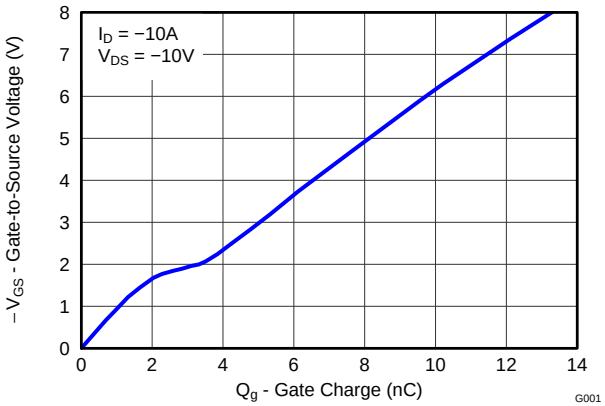


Figure 4. Gate Charge

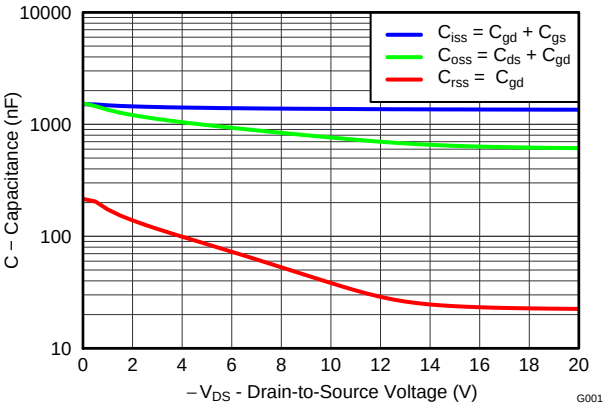


Figure 5. Capacitance

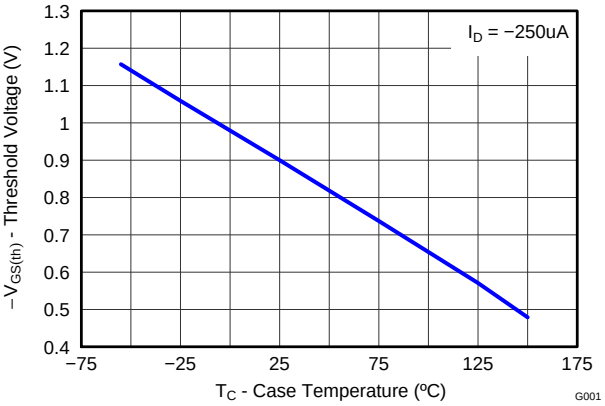


Figure 6. Threshold Voltage vs. Temperature

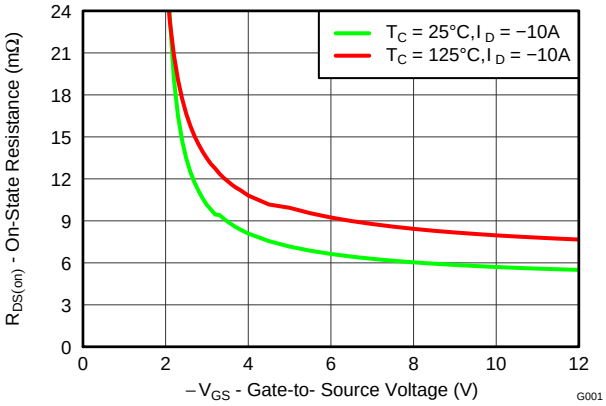


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

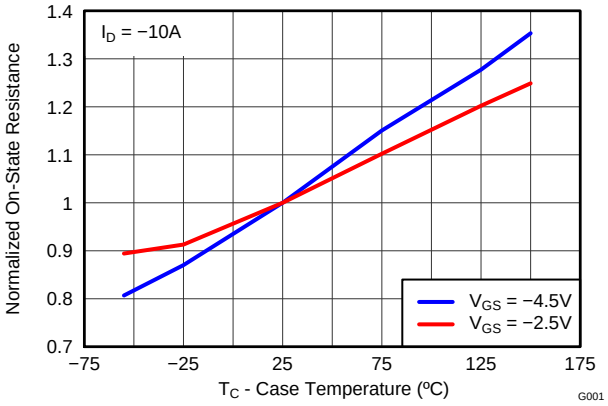


Figure 8. Normalized On-State Resistance vs. Temperature

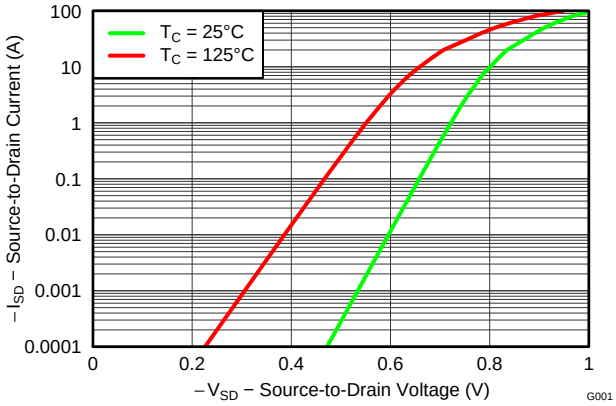


Figure 9. Typical Diode Forward Voltage

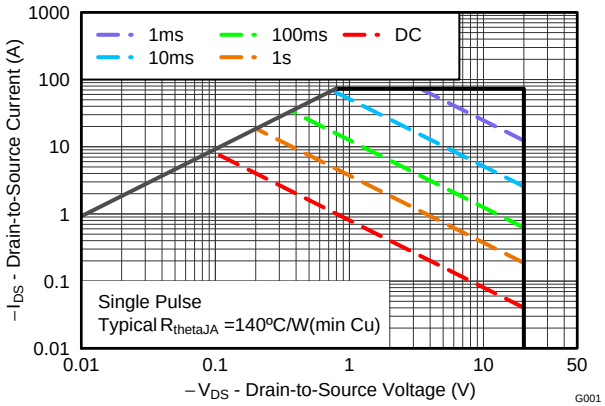


Figure 10. Maximum Safe Operating Area

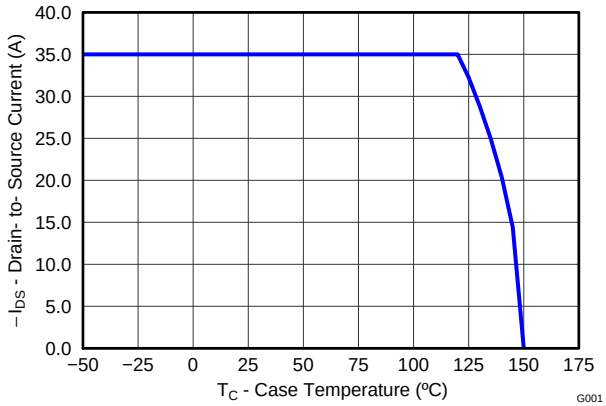
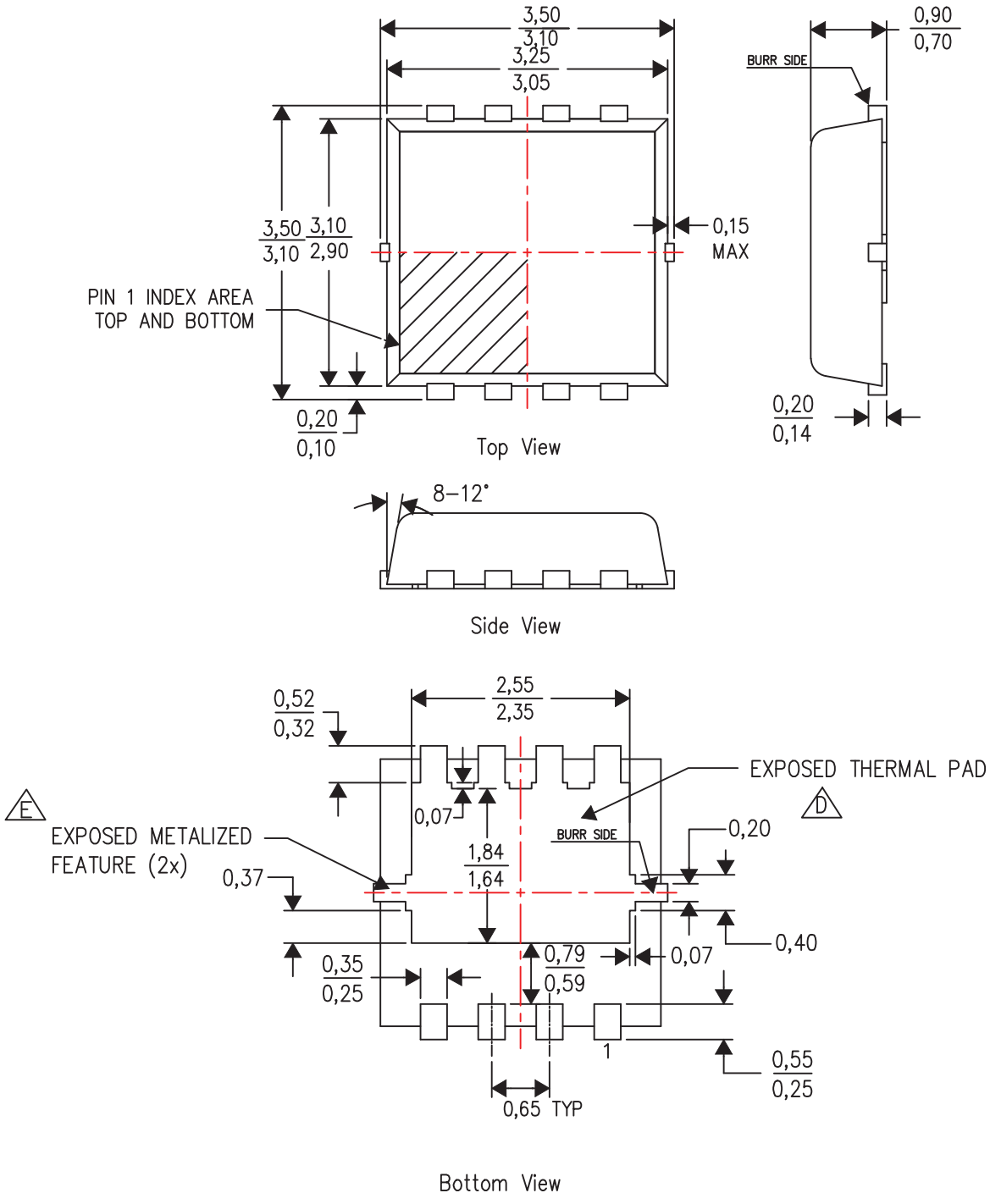


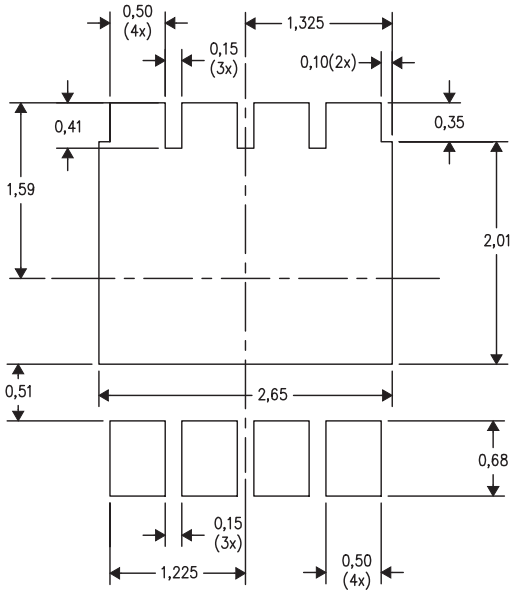
Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q3A Package Dimensions

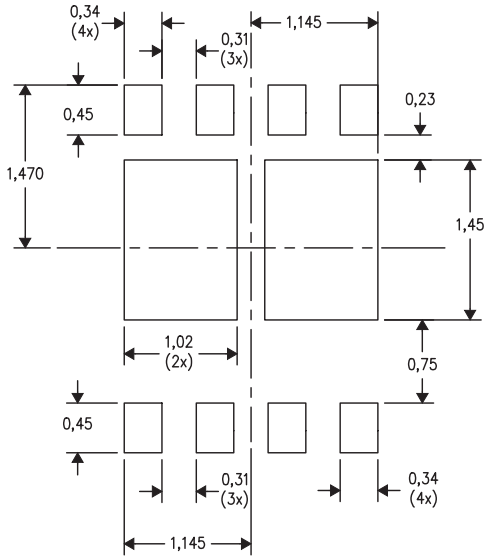


Q3A Recommended PCB Pattern

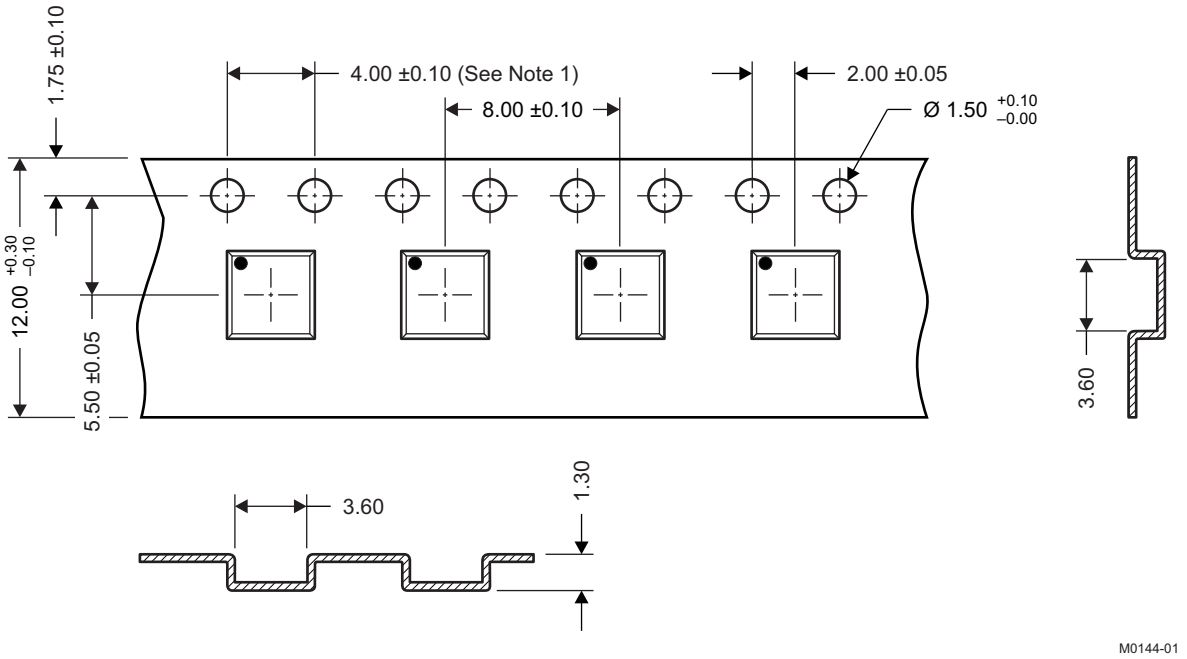


For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q3A Recommended Stencil Pattern



Q3A Tape and Reel Information



Notes:
1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25402Q3A	PREVIEW			8		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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